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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/834,954	04/16/2001	Tomohide Terashima	57454-062	5366

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/834,954	Applicant(s) TERASHIMA, TOMOHIDE
	Examiner Johannes P Mondt	Art Unit 2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,4 and 6-9* is/are allowed.

6)☒ Claim(s) *2,3 and 10-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/31/2003 has been entered.

Response to Amendment

Amendment B filed 11/04/2002 has been entered in response to the abovementioned Request for Continued Examination. Amendment B forms the basis of this office action.

Response to Arguments

The further limitations added to claims 1 and 10, in particular the existence and positioning of a gap directly underneath the second impurity region (of conductivity type opposite to that of the second buried impurity region) has overcome the rejections made under U.S.C. 103(a) of claim 1. However, the rejection under U.S.C. 112, first paragraph, is repeated here, with reference to the comment by examiner in the advisory action of Paper No. 9. Furthermore, the rejection under U.S.C. 103(a) of claims 10-13

over Ito in view of Chevalier is essentially maintained as Ito meets the newly added substantial further limitation, because the buried impurity region has a gap positioned directly underneath the second impurity region 26 (cf. Figure 2(h)).

Claim Objections

1. ***Claim 10*** is objected to because of the following informalities: the verbiage "said second buried impurity region" should be replaced by "said buried impurity region". Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 2-3 and 11 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular: when the third impurity region is stipulated by claims 2 and 11 to be (a) formed on the surface of the semiconductor layer and (b) surrounded by the first impurity region, then it is physically impossible for any electrode parts formed on the surface of said semiconductor layer to be so configured as to cause the first impurity region to be sandwiched between the semiconductor layer and the third semiconductor region. All electrode parts shown by

Applicant are formed on the surface of said semiconductor layer. Claim 3 is also rejected, because it depends on rejected claim 2.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. ***Claims 10 and 12-13*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito (6,051,457) in view of Chevalier (6,291,862). Ito (cf. Figure 2(h) and column 5, lines 1-25) teaches a semiconductor device including: a semiconductor substrate having a main surface; a semiconductor layer of first conductivity type (n type) 32 formed on the main surface of said semiconductor substrate; a buried impurity region of first conductivity type 18 formed between said semiconductor layer and semiconductor substrate; a first impurity region of first conductivity type 34(1) formed on the surface of said semiconductor layer and electrically connected to said buried impurity region (regions 34(1), 32, and 18 abut and are of the same conductivity type, therefore they are electrically connected); a second impurity region of second conductivity type (p type) 26 on the surface of said semiconductor layer located in a region above said buried impurity region; and a semiconductor element which includes said first impurity region and said second impurity region (cf. title and abstract: said semiconductor element being an integrated circuit with passive component and ESD device); and said

buried impurity region includes a gap part wherein said buried impurity region is disconnected (hole or gap filled with impurity region 16(1); column 5, line 16), said gap of said buried impurity region positioned directly beneath said second impurity region.

Ito does not necessarily teach said device to have a switching function and operate in depletion mode. However, Ito does teach in another embodiment a device identical to the one described above as applied to a transistor (cf. Figure 4), while depletion mode transistors are common in the art, as witnessed, among many other available prior art, by Chevalier, who teaches a depletion mode transistor (claims 2, 4, and 42) over a buried well (cf. Figure 7).

With regard to claim 12: the semiconductor element of Ito includes an additional (there are only two impurity regions mentioned in claim 10, so why is this impurity region called "fourth" is puzzling) impurity region 28 of second type formed in the surface of said semiconductor layer.

With regard to claim 13: the gap is in a vertical direction, and any depletion layer normally extends vertically. Therefore, the further limiation of claim 13 does not distinguish over the prior art.

Allowable Subject Matter

4. ***Claims 1, 4 and 6-9*** are allowed. The following is a statement of reasons for the indication of allowable subject matter:

The following prior art considerations are offered in support of allowance of: *claim 1* (and of dependent claims 4 and 6-9):

(a) Ueno (5,895,939) in view of Hwang (EP 0 252 173 A1) teach the semiconductor device of claim 1 except for the circumstance that the gap in the second buried impurity region is positioned NOT directly underneath the second impurity region (64, but instead directly underneath 65). The difference is not obvious over any other prior art found to date.

(b) Farrenkopf et al teach all aspects of claim 1 except the withstand voltage being secured through a depletion that extends from an interface between said second buried impurity region and said semiconductor layer under the condition when the semiconductor element is turned OFF. No mention is made of the depletion layer, a forteriori not about its extent in the vertical direction. No prior art has been found over which the extent of the depletion layer in the vertical direction as required by claim 1 is rendered obvious in Farrenkopf et al. In this regard Ueno is not obvious because the device of Ueno is vertical while the device of Farrenkopf et al is lateral.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
March 5, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800